

Released on May. 28,2009

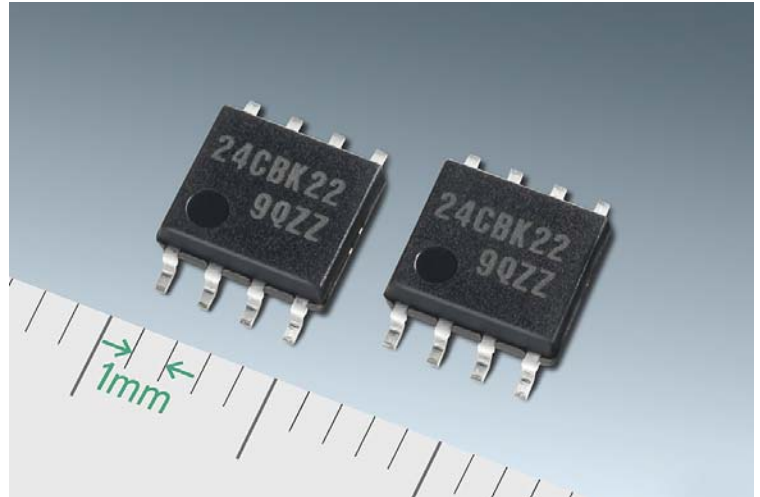
Dual Port EEPROM*2 for EDID*1 Developed

Capable of managing two HDMI*3 terminals with one memory!
Stores Two Sets of EDID Data in One EEPROM.

The number of parts reduced
by half!

LE24CBK22M

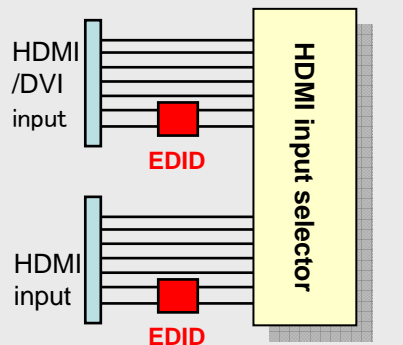
Sample shipment will begin in May 2009.
Production plan : 1,000,000pcs/month
Sample price : 50 yen



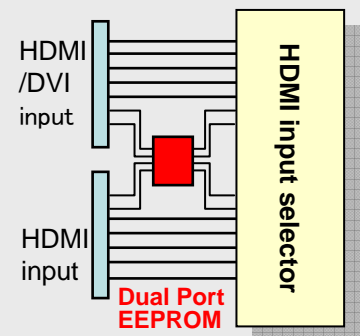
The number of memory parts reduced by half

One LE24CBK22M can read and write from two separate ports, thereby reducing the number of parts, mounting space, and production cost.

The number of parts reduced by half



Conventional method requires one memory chip for each HDMI port.



Using the Dual Port EEPROM makes it possible to deal with two HDMI terminals with one memory.

Existing products can easily be replaced with the Dual Port EEPROM.

As the pin that is normally open on 8-pin general purpose EEPROM is used for the second port interface terminal (SDA/SCL), this product has the same pin configuration as the 8-pin standard EEPROM and is housed in the same compact package.

Existing product can easily be replaced with the new Dual Port EEPROM and writing with general ROM writers is possible. Design changes are easier and investment in equipment can be reduced.

*1 EDID (Extended Display Identification Data): Information for each display such as display resolution and clock type.

*2 EEPROM (Electrically Erasable and Programmable Read Only Memory): Electrically erasable programmable read-only memory

*3 HDMI (High-Definition Multimedia Interface): Interface standard for image-output terminal installed in digital image device.

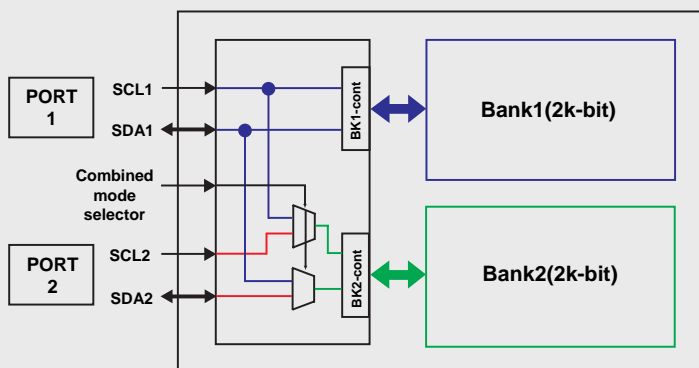
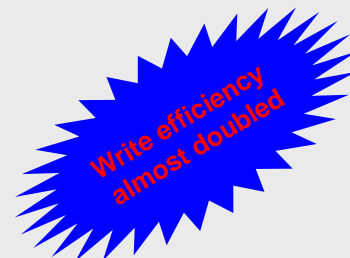
Since it outputs digital signal without any change, video data will not be degraded.

*The information presented in this product topics, including device specifications, is current as of the date of the press release.

Note, however, that this information is subject to change without notice and thus at later dates the current state may differ in certain details from the content presented here.

Includes combined mode

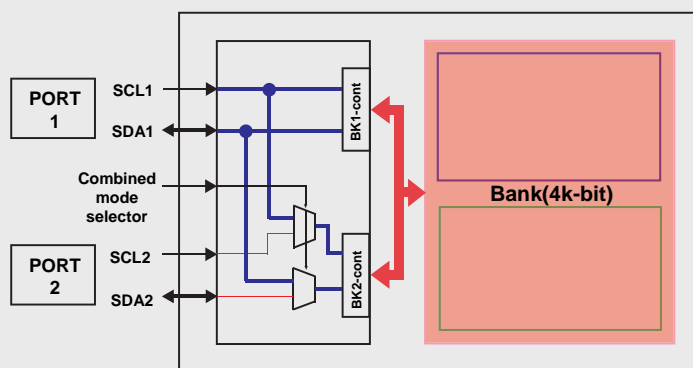
In combined mode operation, the memory area of the two separate ports operates as combined one sequential memory area for writing. This enables to write 4 Kbit display information for two terminals at the same time, without configuring each memory area for writing, which contributes to a significant increase in work efficiency.



During normal mode operation, Bank1 (2 Kbit) memory region in which reading and writing are performed through SCL1/SDA1 and Bank2 (2 Kbit) memory region in which reading and writing are performed through SCL2/SDA2 are handled separately. Equivalent operation of two memories for EDID is possible with one Dual Port EEPROM.

At operation usually

Combined mode operation is available during the writing operation. Bank1 (2 Kbit) memory region and Bank2 (2 Kbit) memory region are integrated and treated as one memory of 4 Kbit thus reducing the writing time. Writing is performed through the SCL1/SDA1 ports. Writing with general ROM writers is possible.



Write operation in combined mode

Specifications

- Capacity : 2kbit(256 x 8bit) + 2kbit(256 x 8bit) total 4kbit
- Bank composition : 2bank (2kbit + 2kbit)
- Supply voltage : 2.5V to 5.5V
- interface : Two wire serial interface (I²C DDC2)
- Maximum operating clock frequency : 400kHz
- Low power consumption : During standby 2uA(max), During reading 0.5mA(max)
- page write mode : 16 Byte
- read mode : Sequential read and random read
- Erase/Write cycles : 10⁶ cycles
- Adopts SANYO's proprietary symmetric memory array configuration (USP6947325).